VHDL Introduction and Overview

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What is VHDL?

- Very-High-Speed Integrated Circuit Hardware Description Language
- VHDL appeared in 1983
- VHDL was sponsored by US Department of Defense
- VHDL borrowed heavily from Ada programming language
- Formal definition of VHDL was given by IEEE Standard VHDL Language Reference Manual

What is the original intent of inventing VHDL?

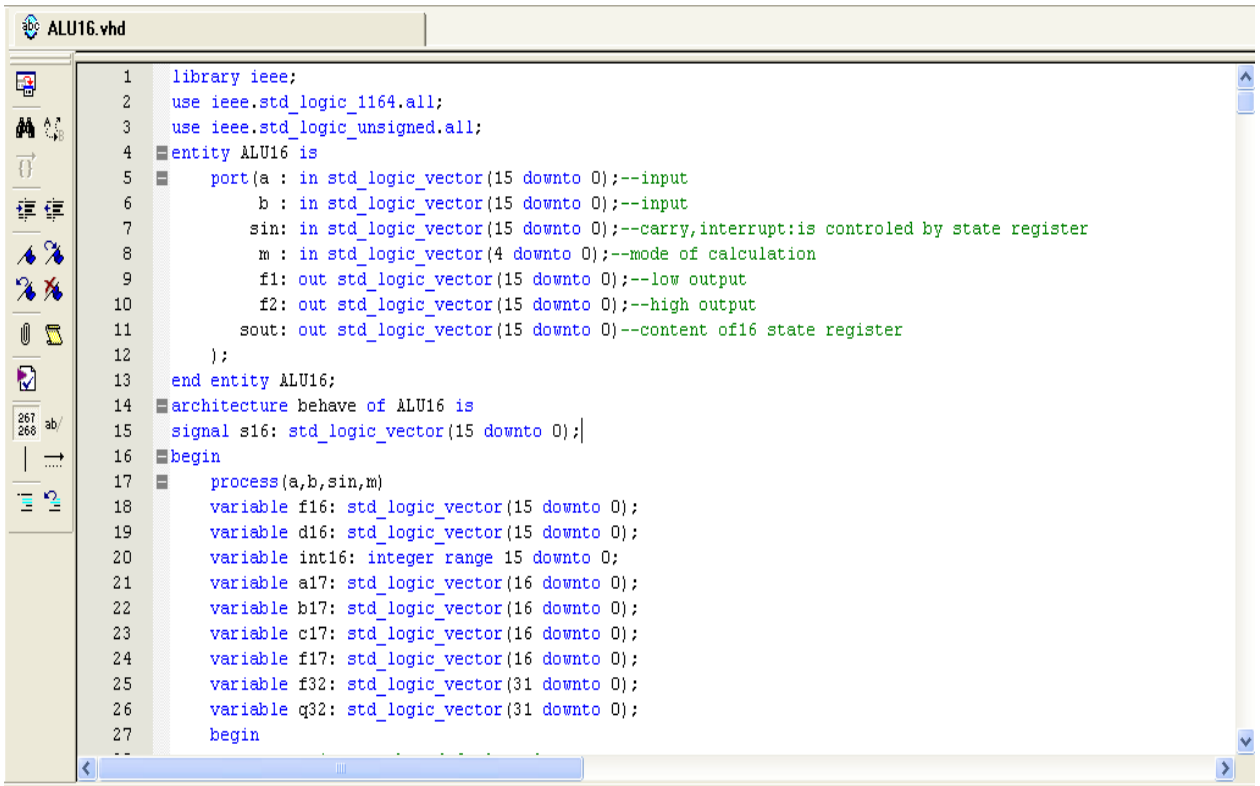
- Serve as a means of communicating designs from one contractor to another in the very high speed integrated circuit program
- CDL,ISP,and AHPL have been used since 1970s

VHDL Design Tools & Products

- Textual Editor
- Schematic Editor
- Simulators
- Checkers and Analyzers
- Optimizers and Synthesizers
- FPGA

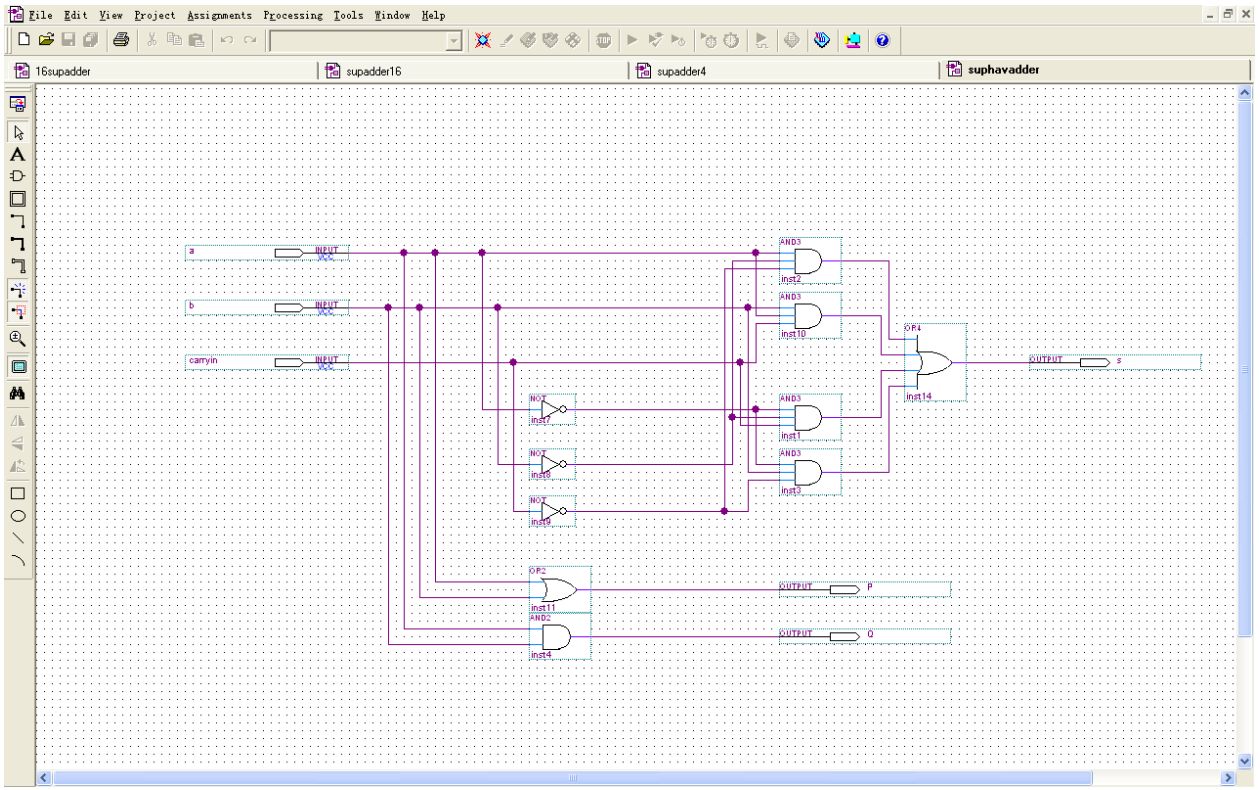
Textual Editor

- An editor can be used to edit VHDL source code.



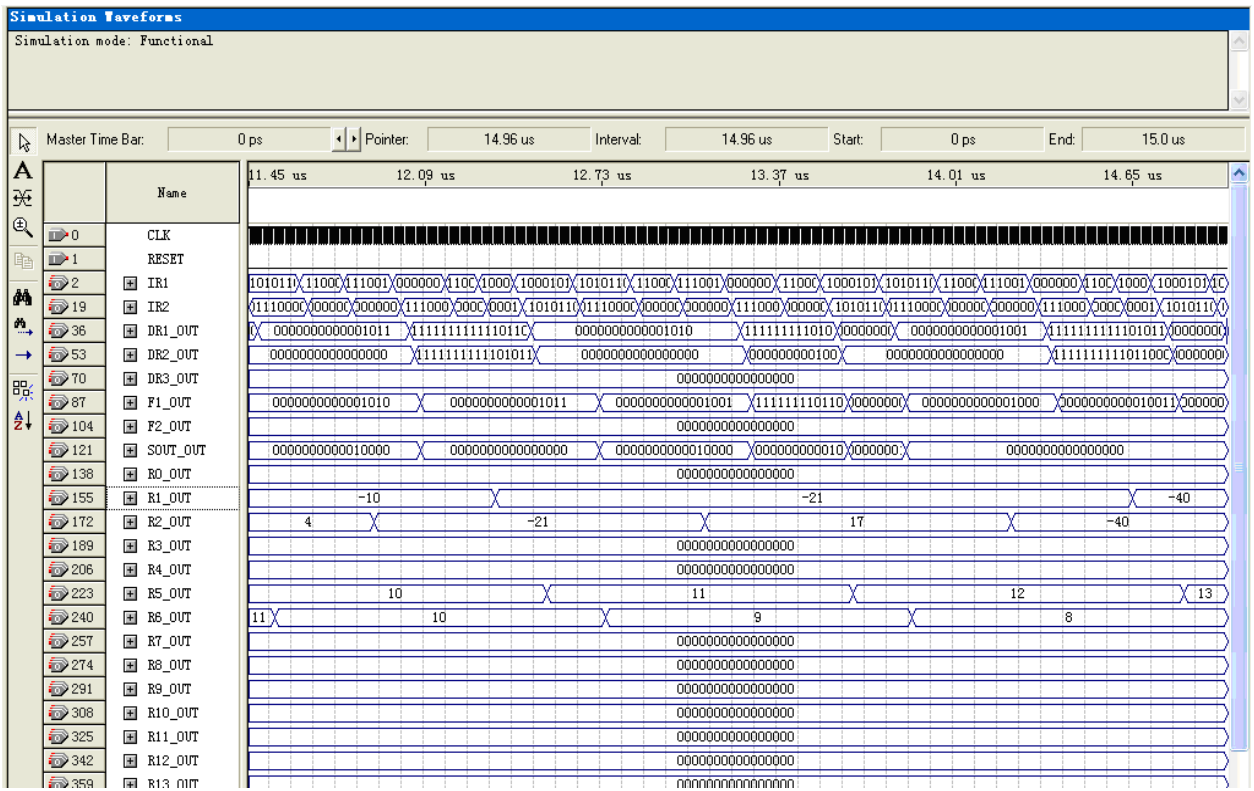
Schematic Editor

- An editor which can be used to create and display an interconnected set of graphic tokens.



Simulators(Soft Logic Analyzer)

- A hardware debugger which models the response of a system to input stimuli.



Checkers

- Rule checkers
  At the silicon level, design rule checkers are used to insure that the layout implies a circuit that can be fabricated reliably.
  At other levels, rule checkers are used to determine if connection rules or fanout rules have been violated.

Analyzers

- Analyzers
  Timing analyzers can be used to check for errors that violate the structure and meaning of the language and also can be used to check for the longest path through a logic circuit or system.

Optimizers

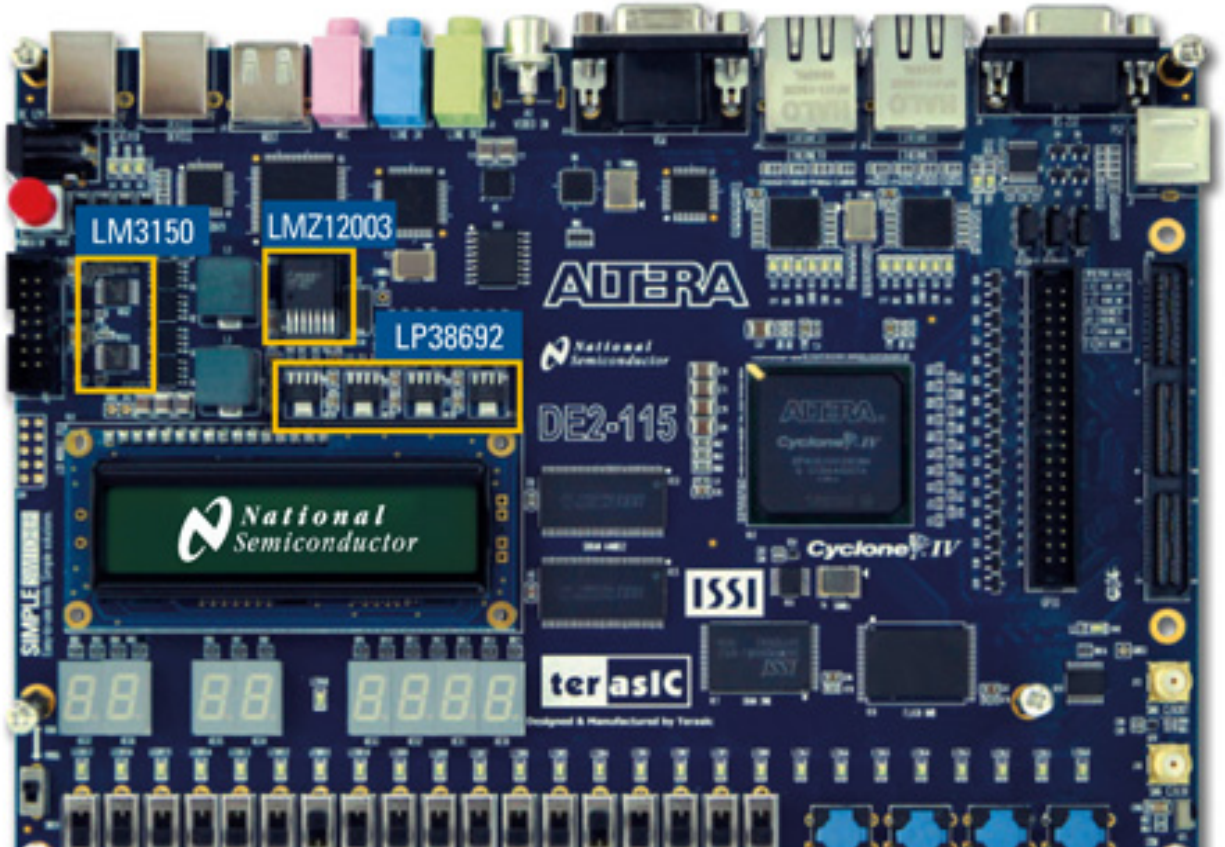
- Optimizers
  Optimizers change the form of the design representation to a new form,which is regraded as "improved" in some fashion.
  For example,at register level,optimizers are used to determine the best combination of control sequence and data paths.

Synthesizers(Silicon Compiler)

- Synthesizers
  A high-level synthesizer translates a representation of a circuit at a high level of abstraction into a lower-level representation that can be implemented within a particular technology.

What is FPGA?

- Field Programmable Gate Array
- FPGAs can be used to implement any logical function specified by a hardware description language



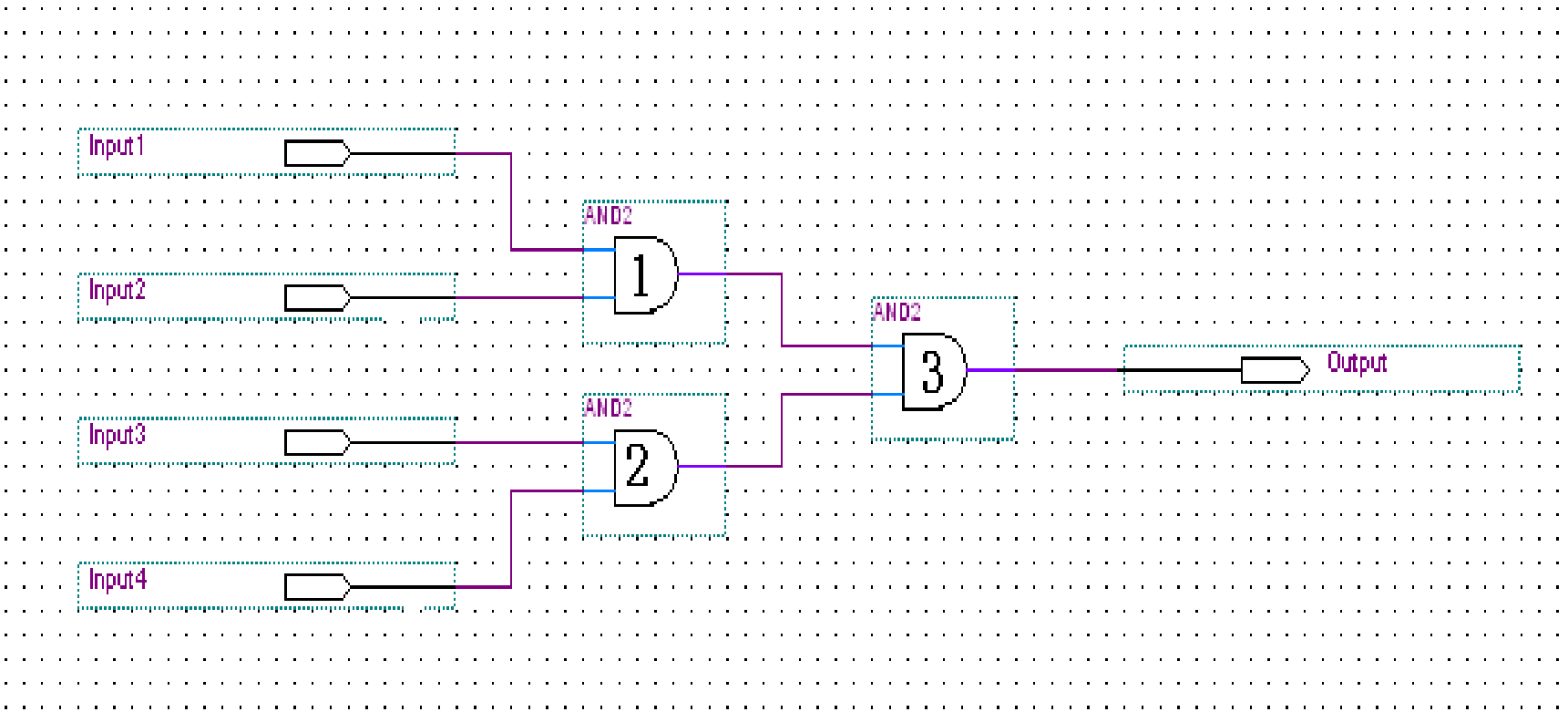
Language Constructs of VHDL

- Language Constructs Similar to C Programming Language
- Language Constructs Specified for Modeling Hardware Circuits

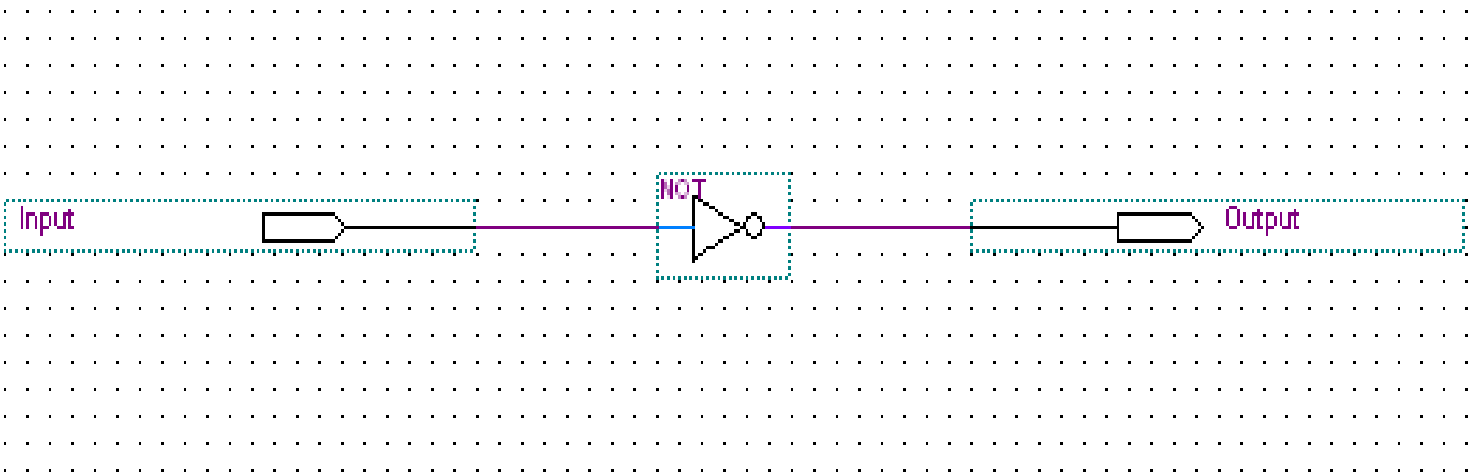
Features of Digital Circuit

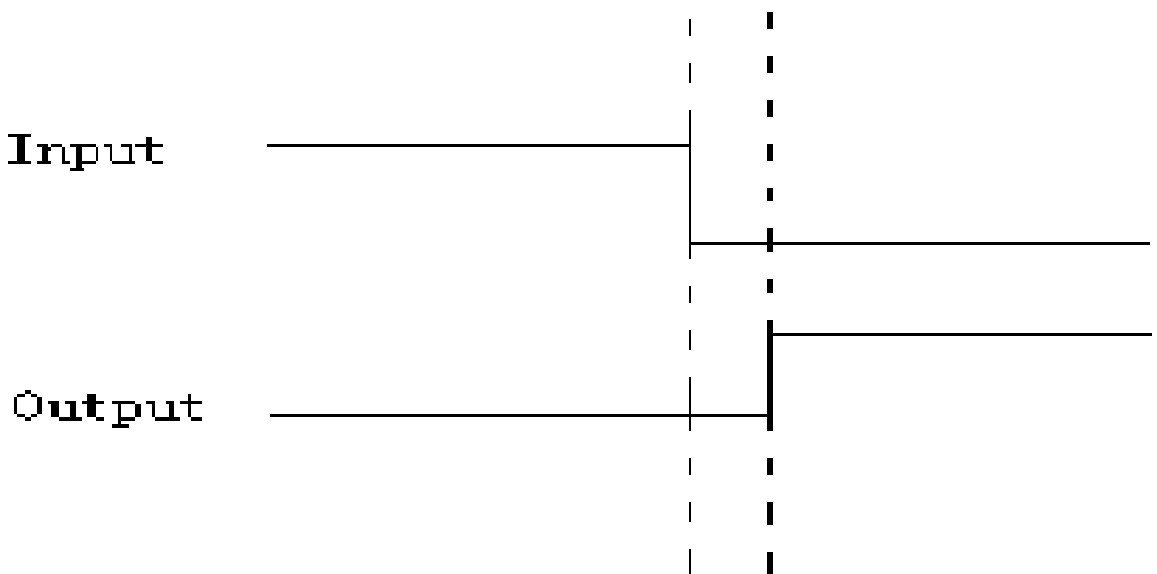
- Concurrency
- Delay
- Timing

Concurrency

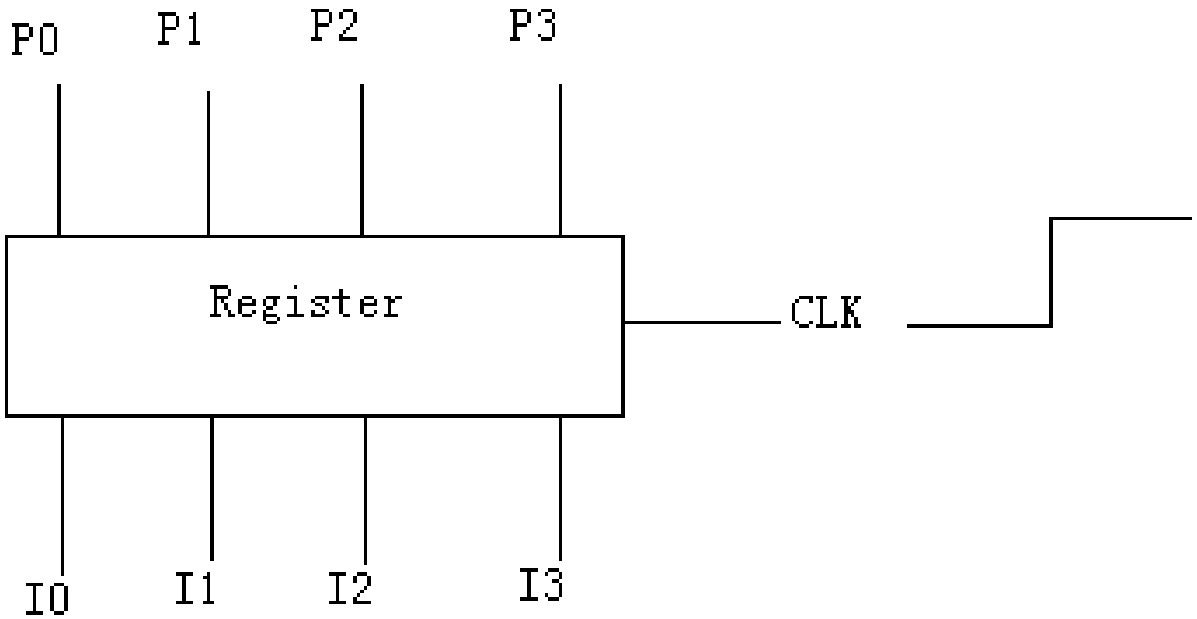


Delay

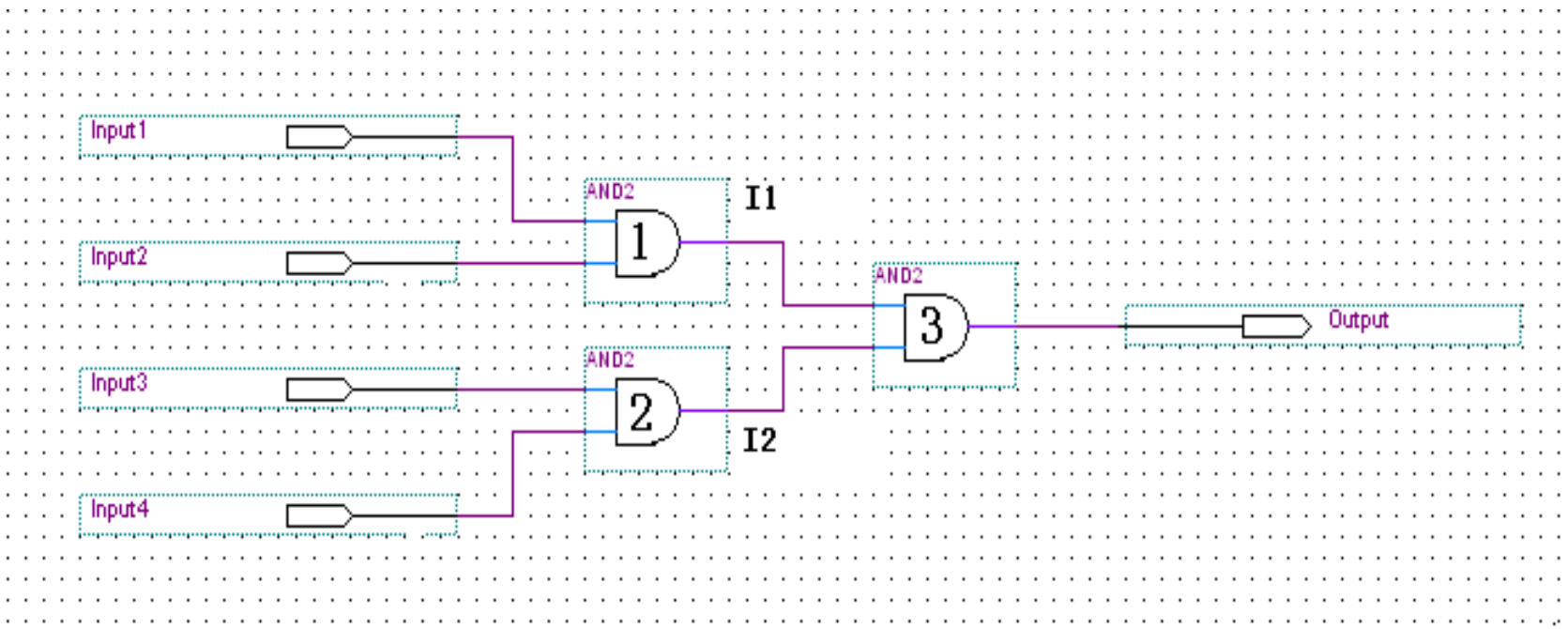




Timing

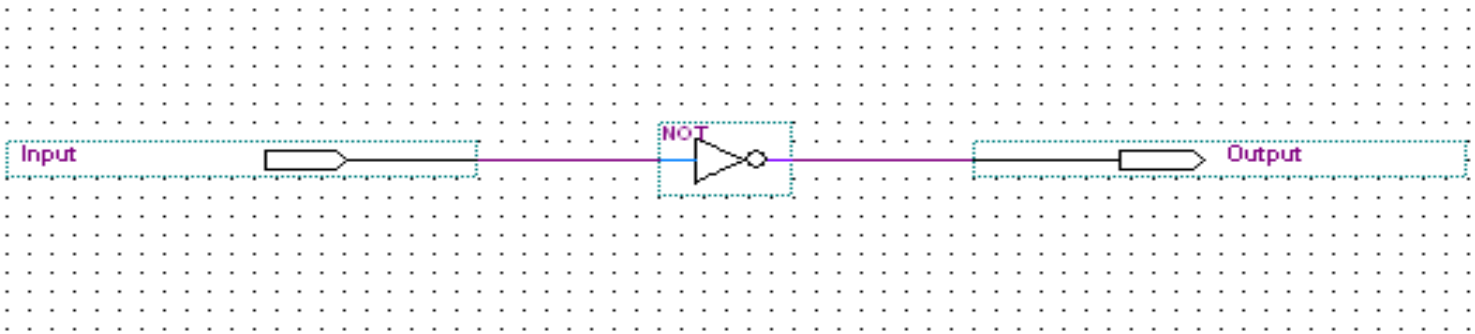


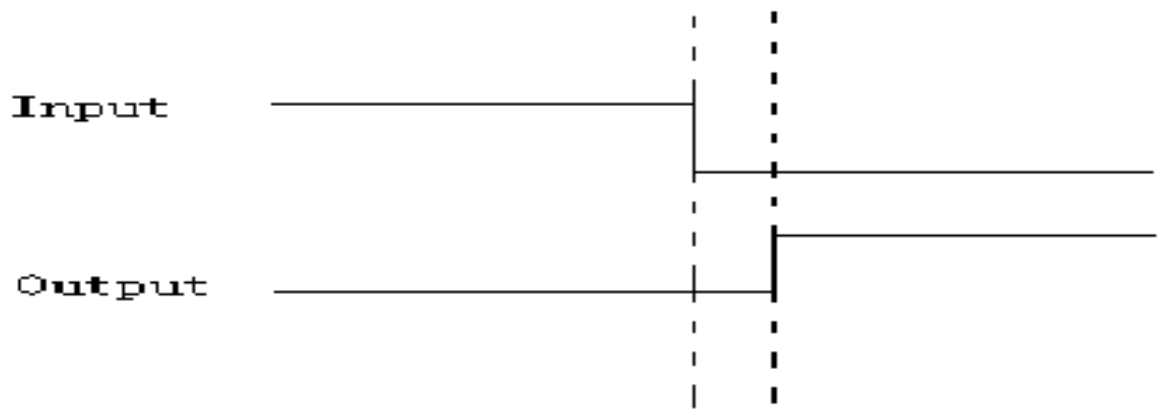
Concurrent Mechanism in VHDL




```
architecture one of concurrent is
  signal I1 : BIT;
  signal I2 : BIT;
    begin
      output <= I1 and I2;
      I2 <= Input3 and Input4;
      I1 <= Input1 and Input2;
end one;
```

Delay Mechanism in VHDL

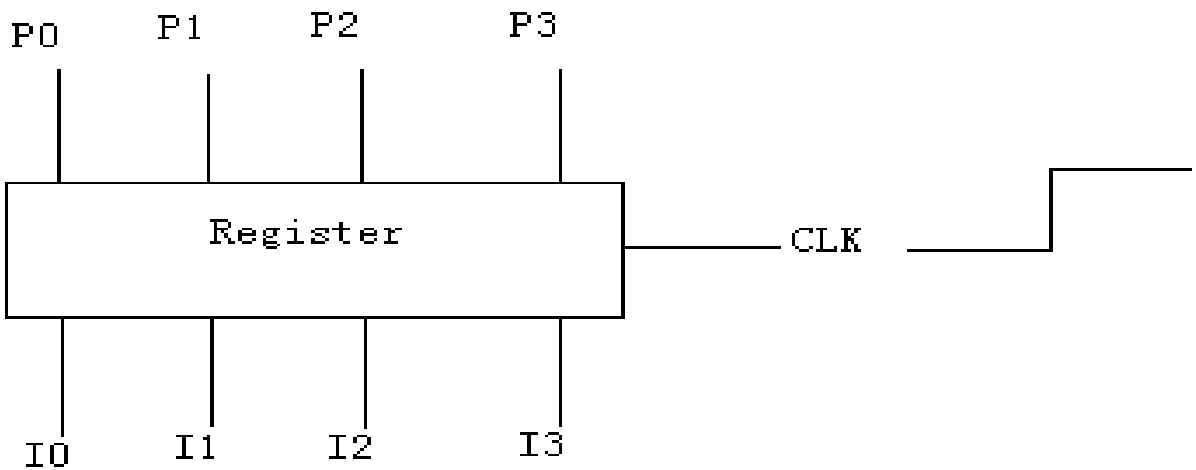





```
Output <= not Input after 5 ns;

Output <= not Input; after delta time by default
```

Timing Mechanism in VHDL




```
if (clk'event and clk='1') then
  P[3..0] <= I[3..0];
end if;
```

Signal

- Signals are used to represent data values on actual physical data lines in circuits.
- Logic Value of Signal

```
Type MVL4 is ( 'X ', – unknown
               '1' , – logic 1
               '0' , – logic 0
               'Z' ); –high impedance

Type MVL7 is ( 'X ', – strong X (strong unknown)
               '1' , – strong 0 (strong low)
               '0' , – strong1 (strong high)
               'Z' , – tri-gate X (high impedance)
               'W', – weak X (weak unknown)
               'L' , – weak 0 (weak low)
               'H' ); – weak 1 (weak high)
```

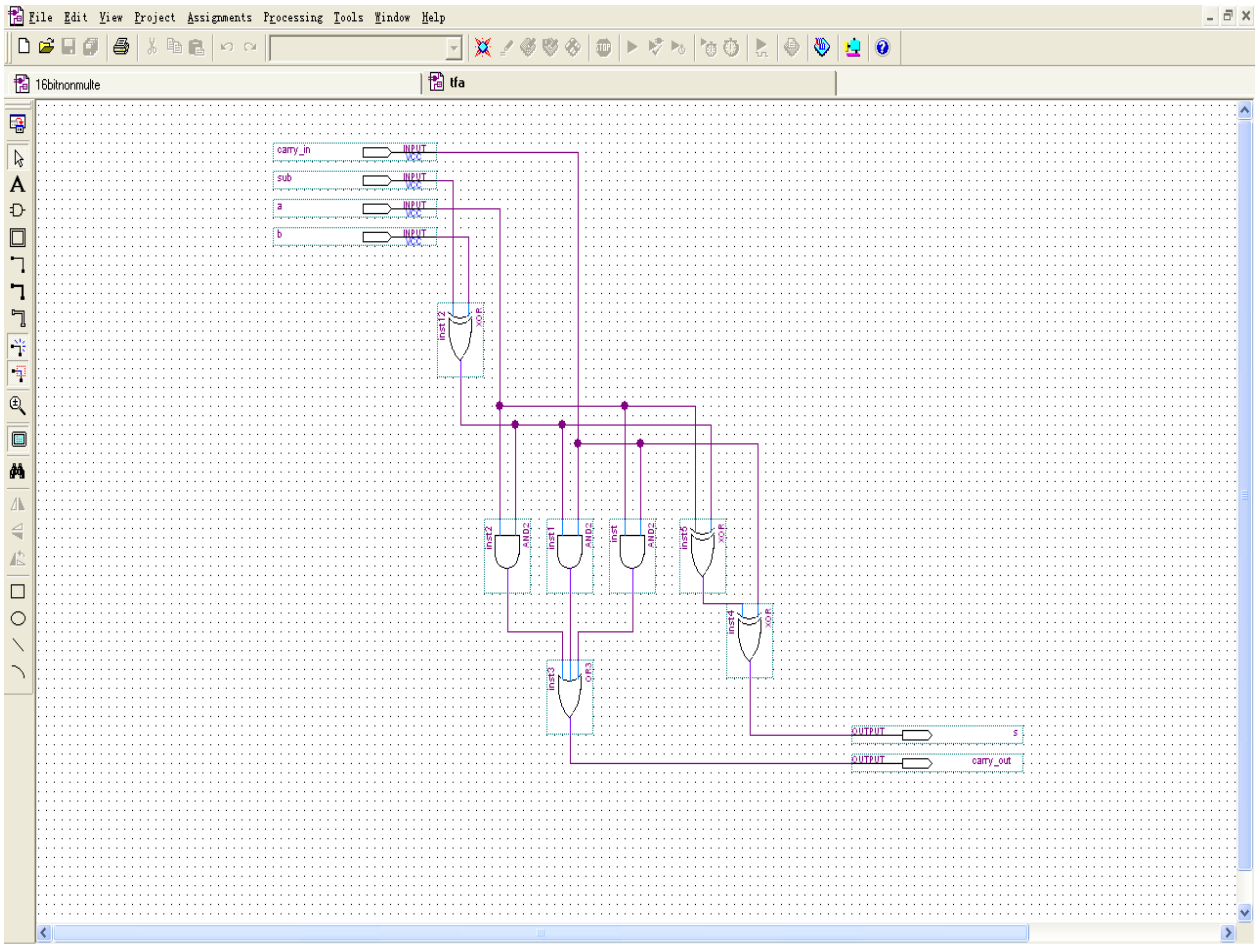
16-bit Multiplier Designed by VHDL

- VHDL Source Code
- entity Multiplier_VHDL is

```
port ( Input1, Input2: in std_logic_vector(15 downto 0);
Result: out std_logic_vector(31 downto 0) );
end entity Multiplier_VHDL;
architecture Behavioral of Multiplier_VHDL is
begin
Result <= std_logic_vector(unsigned(Input1) * unsigned(Input2));
end architecture Behavioral;
```

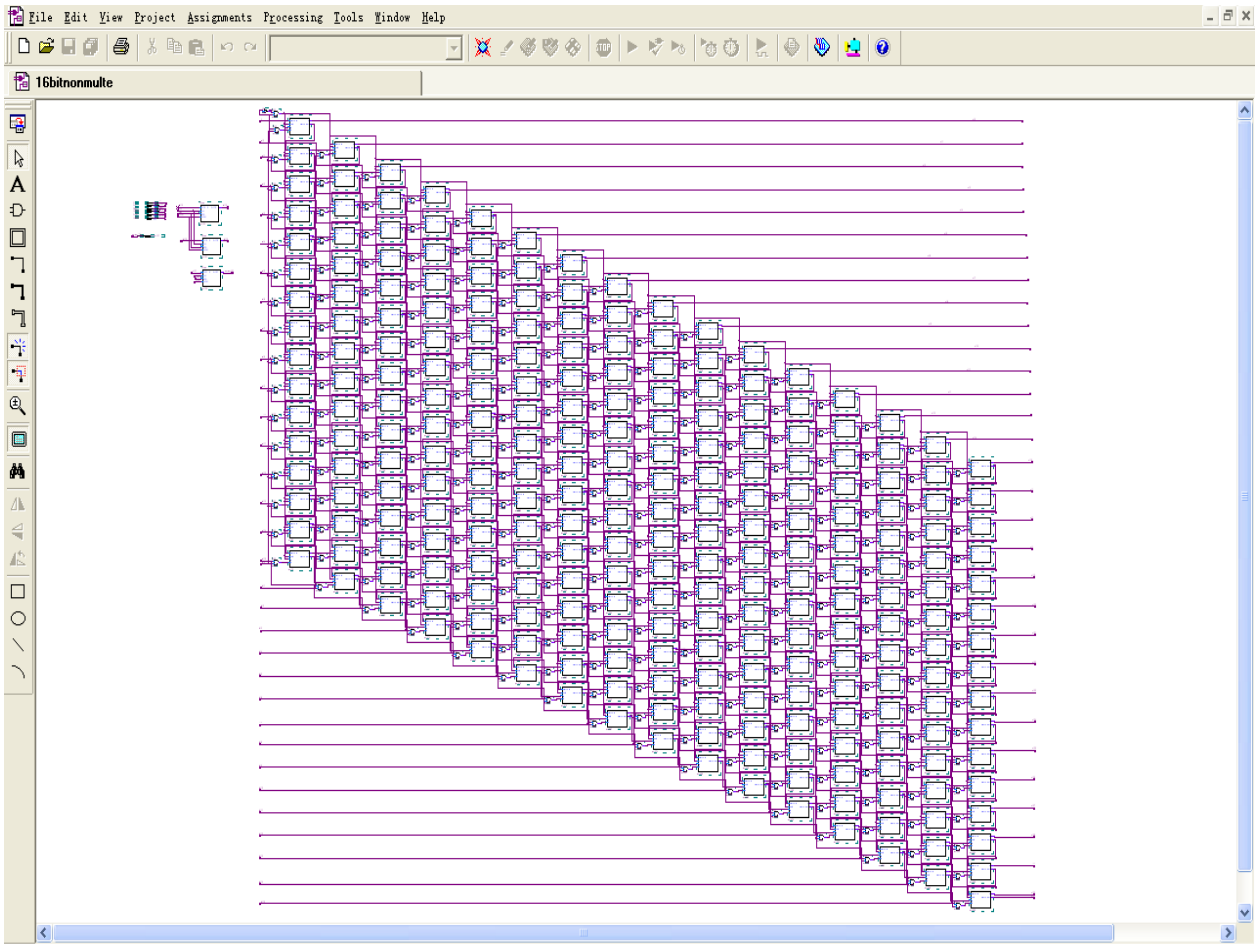
16-bit Multiplier Designed by Schematic

- Schematic Representation(Part I)



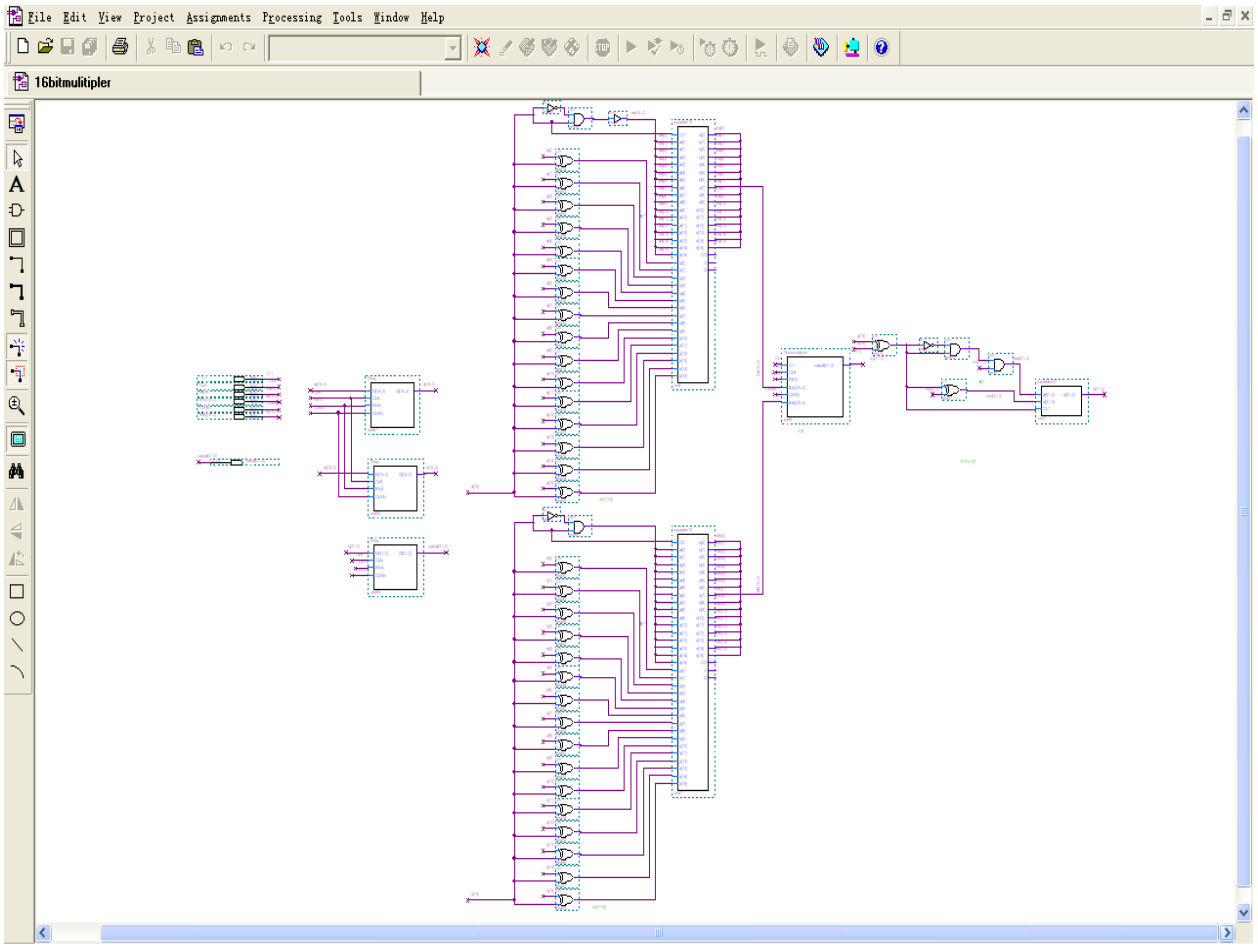
16-bit Multiplier Designed by Schematic

- Schematic Representation(Part II)



16-bit Multiplier Designed by Schematic

- Schematic Representation(Part III)



Advantages of VHDL on Hardware Design

- Public Design Platform
- Intellectual Property Core
- Logical and Timing errors are basically eliminated before building real hardware
- Line between hardware and software become unclear

Shortcoming

- Long synthesize time
- Synthesizer may make a mistake
- Tool for computing longest path through a circuit is not perfect

References

- A VHDL PRIMER (Third Edition)
  Author:Jayaram.Bhasker
- VHDL Design Representation and Synthesis (Second Edition)
  Author:James R.Armstrong,F.Gail Gray

Thanks!