ECE4740: Digital VLSI Design

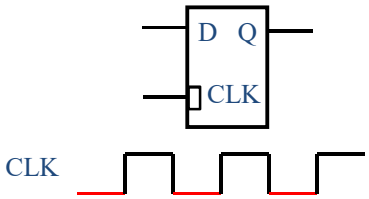
Lecture 17: Sequential circuits

Still important!

Timing recap

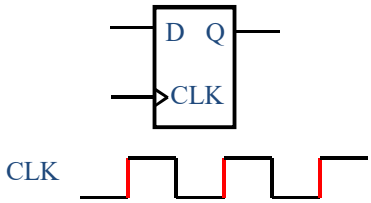
Latch vs. flip-flop

- Latch
  - Stores data when CLK signal is low



  - Level sensitive

- Register/flip-flop
  - Stores data when CLK signal rises



  - Edge sensitive

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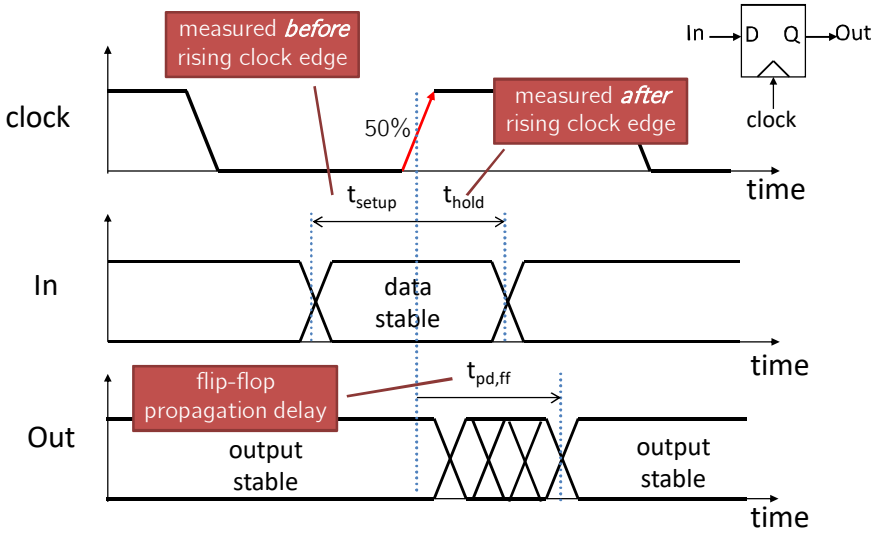
Setup time, hold time, & propagation delay



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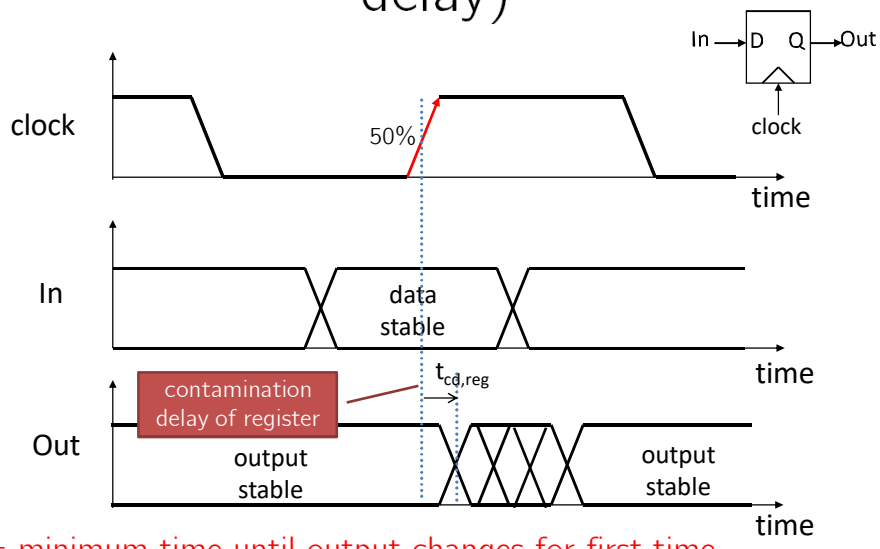
Contamination delay (or min-delay)



= minimum time until output changes for first time

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You will need a lot of practice

Timing examples

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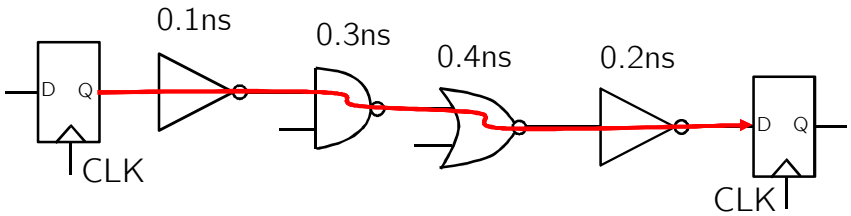
Simple timing example



- What is the minimum clock period T?
  - $t_{setup,ff}$=0.2ns, $t_{hold,ff}$=0.2ns, $t_{pd,ff}$=0.3ns
- $t_{pd,logic}$=0.1+0.3+0.4+0.2=1.0ns
- $T \geq t_{pd,ff}+t_{pd,logic}+t_{setup}$=1.5ns → f_{max}=666MHz

if static CMOS is used, anything lower also works!

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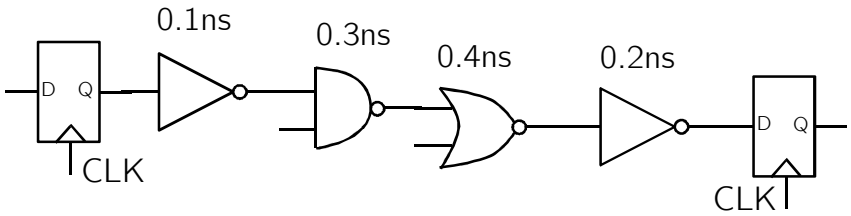
Simple timing example (cont'd)



- What is the minimum clock period T?
  - t_{setup}=0.2ns, t_{hold}=0.2ns, $t_{pd,ff}$=0.3ns
- Check hold condition: $t_{cd,ff}+t_{cd,logic} \geq t_{hold}$
- Need to know contamination delays!

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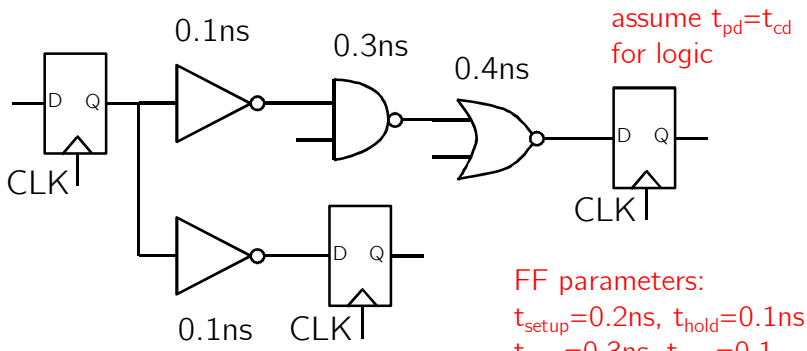
Your turn: simple circuit



- What is the max. clock frequency
- Will the circuit work (hold condition)?

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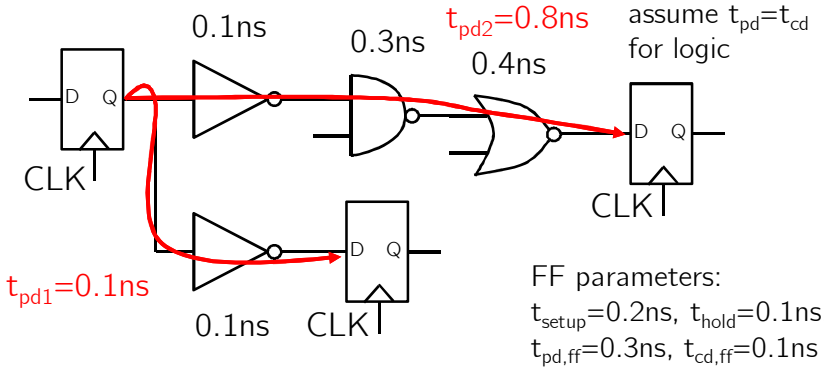
Solution: simple circuit



- Find critical path = path that determines f_{clk}
- t_{pd2}=0.8ns

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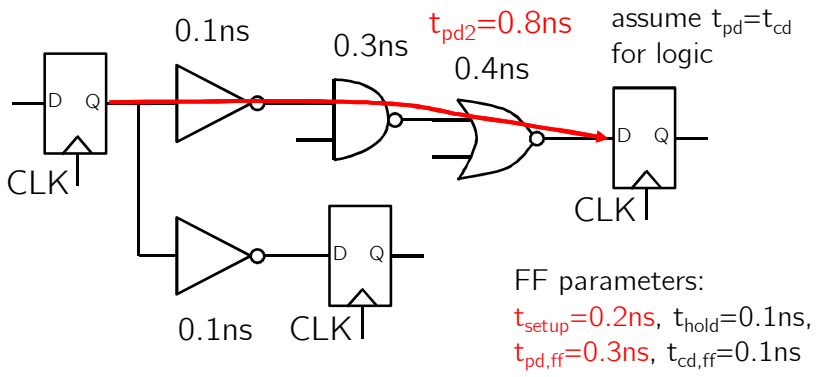
Solution: simple circuit (cont'd)



- Compute T_{min}=$t_{pd,ff}$+t_{pd2}+t_{setup}=1.3ns
- Max clock frequency: 769MHz

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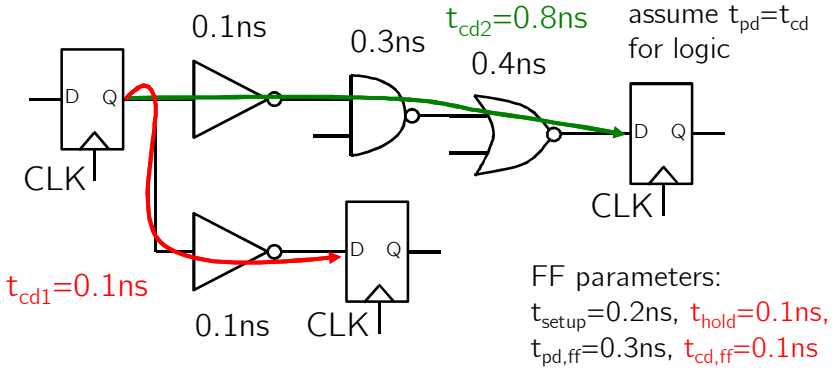
Solution: simple circuit (cont'd)



- Never forget to check the hold conditions
- $t_{cd,ff}$+$t_{cd,logic}$≥t_{hold} → 0.1ns+0.1ns≥0.1ns ✓

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Important

- Setup violations can usually be resolved by reducing the clock frequency (increasing T)
  - Fixed after chip manufacturing
- Hold violations cannot be resolved by altering the clock frequency
- Hold violations have to be resolved at design time (insert logic, skew clocks, etc.)
  - In some cases, you can reduce the temperature by a lot, but that's not practicable at all

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Happens in all sequential circuits

Clock skew

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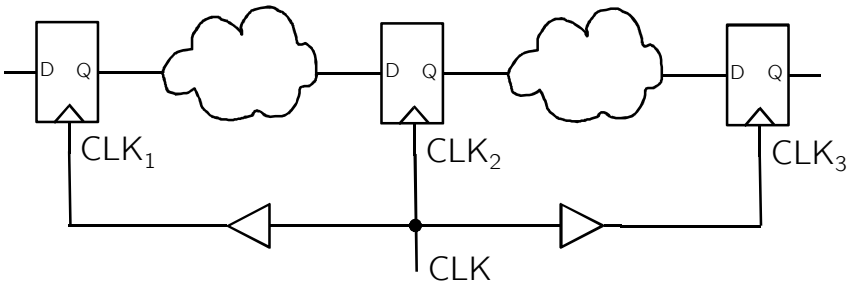
Clock skew*



- CLK signal often have different time offsets (or arrival times) at each flip-flop input

*reasons: clock tree, buffers, wire lengths, fan out, etc.

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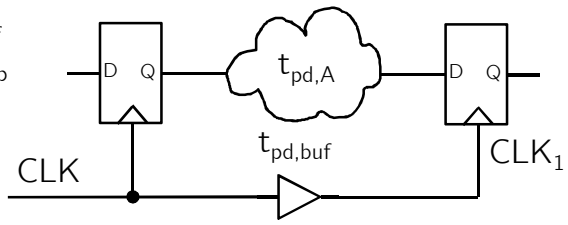
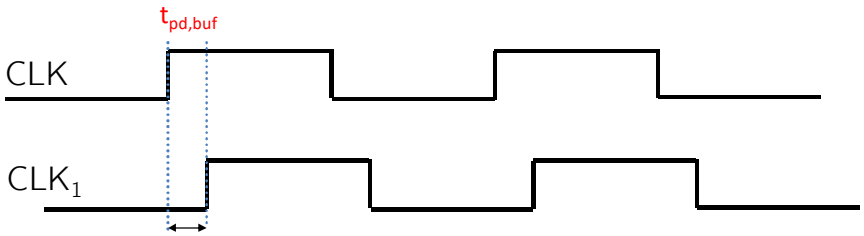
Clock skew affects timing!

- $t_{pd,ff}$
- t_{setup}
- t_{hold}





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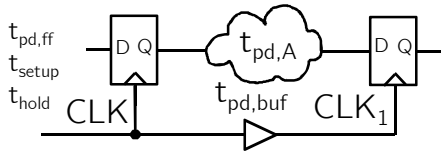
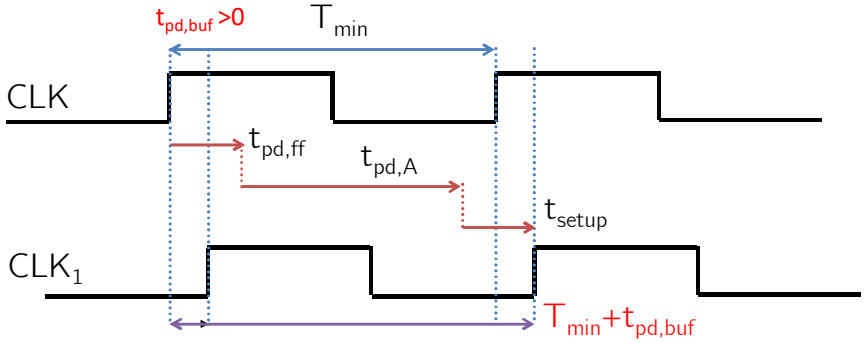
Impact on minimum clock period



so-called useful skew!

$T_{min}+t_{pd,buf}=t_{pd,ff}+t_{pd,A}+t_{setup}$



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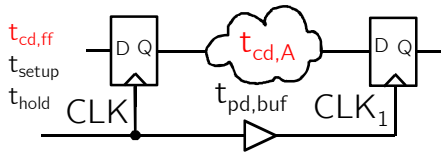
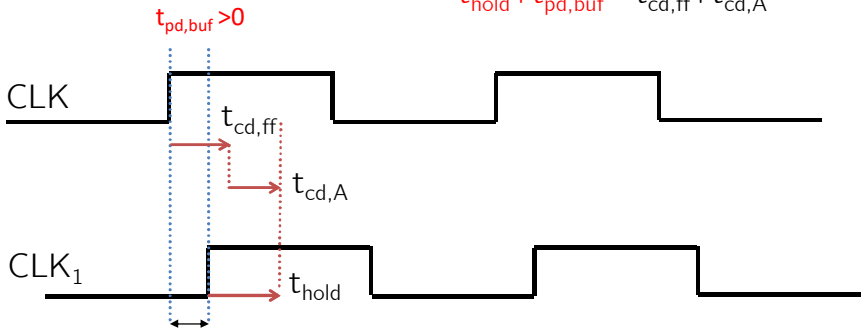
Impact on hold condition



hold condition often gets worse with clock skew

$t_{hold}+t_{pd,buf} \leq t_{cd,ff}+t_{cd,A}$



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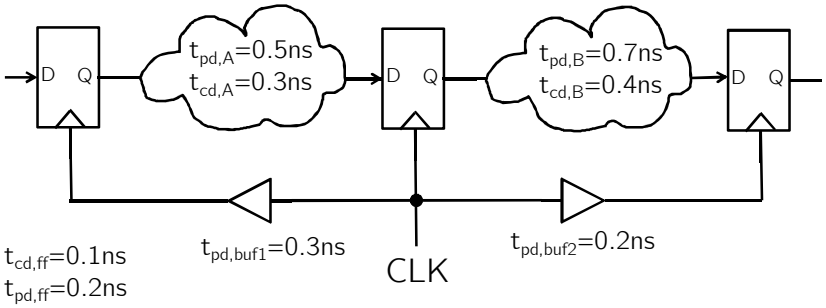
Your turn: timing with clock skew



$t_{cd,ff}$=0.1ns
$t_{pd,ff}$=0.2ns
t_{setup}=0.2ns
t_{hold}=0.2ns

- What is the maximum clock frequency?
- Will the circuit work?

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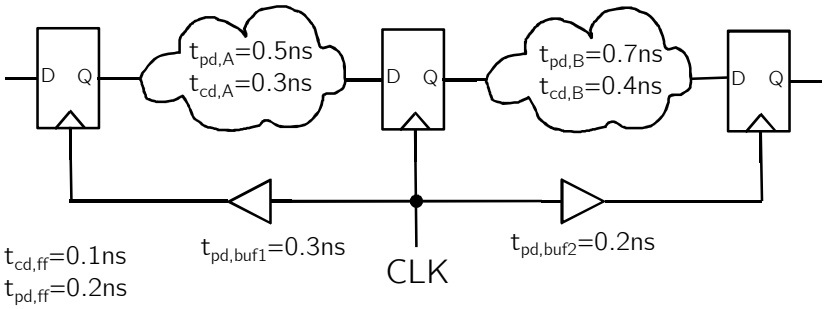
Maximum clock frequency



$t_{cd,ff}$=0.1ns
$t_{pd,ff}$=0.2ns
t_{setup}=0.2ns
t_{hold}=0.2ns

negative clock skew reduces speed

f_{max}=1/1.2ns=833.3MHz

- $T_{min1} - t_{pd,buf1} = t_{pd,ff} + t_{pd,A} + t_{setup}$ → T_{min1}=1.2ns
- $T_{min2} + t_{pd,buf2} = t_{pd,ff} + t_{pd,B} + t_{setup}$ → T_{min2}=0.9ns

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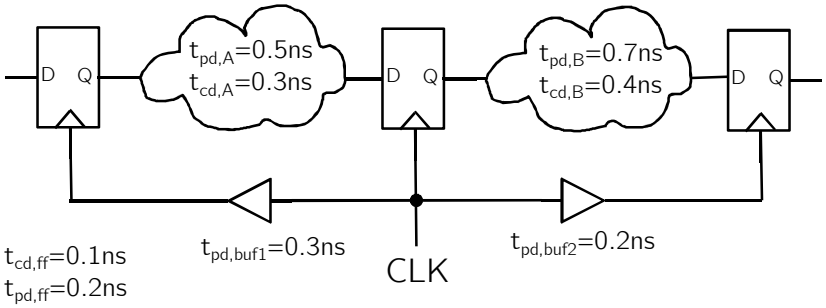
Check hold condition



negative clock skew relaxes hold condition

- $t_{hold}-t_{pd,buf1} \leq t_{cd,ff}+t_{cd,A}$ → met!
- $t_{hold}+t_{pd,buf2} \leq t_{cd,ff}+t_{cd,B}$ → met!

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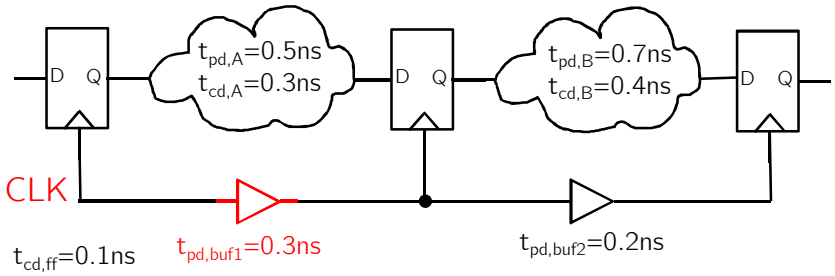
Check hold condition (cont'd)



remains unchanged!

- $t_{hold}+t_{pd,buf1} \leq t_{cd,ff}+t_{cd,A}$ → not met!
- How about the 2nd hold condition?

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Clock skew and timing summary

- Clock skew happens in all VLSI circuits
- Clock skew can be useful or not in terms of maximum clock frequency or hold condition
- Draw clocks & timing conditions on paper for manual analysis
- VLSI design tools (e.g., Synopsys DC) are good at reporting and resolving timing issues
- Simulate circuit in all process corners
  - Worst case → max. clock frequency
  - Best case → check hold condition

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